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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,038	08/04/2003	Howard E. Castle	2000.107300	5836

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EXAMINER	
KOSOWSKI, ALEXANDER J	

ART UNIT	PAPER NUMBER
2125	

DATE MAILED: 03/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/634,038	CASTLE ET AL.	
	Examiner	Art Unit	
	Alexander J Kosowski	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1) Claims 1-28 are presented for examination.

Claim Rejections - 35 USC § 102

2) The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3) Claims 1-4, 6, 10-12 and 14 are rejected under 35 U.S.C. 102(e) as being unpatentable by Patel et al (U.S. Pat 6,584,369).

Referring to claim 1, Patel teaches a method, comprising: identifying at least one wafer to be processed (col. 3 lines 5-6), identifying a process tool in which said at least one wafer is to be processed (col. 4 lines 10-19); obtaining enhanced metrology data regarding a process operation to be performed in said identified process tool prior to processing said identified at least one wafer in said identified process tool (col. 3 lines 19-45, whereby feedback data containing any equipment disturbances is considered enhanced data); and positioning said at least one wafer in said identified process tool and performing said process operation thereon (col. 5 lines 11-27).

Referring to claim 2, Patel teaches the method of claim 1, further comprising, prior to performing said process operation in said identified process tool, analyzing at least said enhanced metrology data to determine if said process tool is acceptable for processing said identified at least one wafer (col. 3 lines 5-18).

Referring to claim 3, Patel teaches the method of claim 1, wherein said identified at least one wafer is part of a lot of wafers identified for processing in said identified process tool (col. 3 lines 5-6).

Referring to claim 4, Patel teaches the method of claim 1, wherein said identified at least one wafer is a wafer wherein production integrated circuit devices are formed thereon (col. 2 lines 53-64, whereby semiconductor wafers are processed).

Referring to claim 6, Patel teaches the method of claim 1, wherein said identified process tool is at least one of a deposition tool, an etch tool, a furnace, an ion implant tool, a chemical mechanical polishing tool and a photolithography tool (col. 4 lines 55-63).

Referring to claim 10, the claim varies from claim 1 in that it claims a lot of wafers rather than at least one wafer. Patel teaches that lots of wafers may be processed (col. 3 lines 5-6). Therefore, referring to claim 10, see the rejection of claim 1 above.

Referring to claim 11, see rejection of claim 2 above.

Referring to claim 12, see rejection of claim 4 above.

Referring to claim 14, see rejection of claim 6 above.

Claim Rejections - 35 USC § 103

4) The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5) Claims 7-9, 15-20, 22-26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel, further in view of Shanmugasundram et al (U.S. PGPUB 2002/0193899).

Referring to claims 7-9, Patel teaches the above. However, Patel does not explicitly teach that the step of obtaining enhanced metrology data regarding said process operation comprises obtaining a greater amount of metrology data for said process operation relative to an amount of metrology data obtained for said process operation, obtaining a different type of metrology data for said process operation relative to a type of metrology data obtained for said process operation, nor increasing a frequency at which metrology data for said process operation is acquired relative to a frequency at which metrology data for said process operation is acquired, in accordance with a previously established metrology sampling plan.

Shanmugasundram teaches a method for dynamically altering sampling schemes in a semiconductor processing environment whereby different sampling frequencies, different types of data and different amounts of sampling can be varied in order to provide enhanced metrology data (Paragraph 0015 and Paragraphs 0037-0039).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to utilize different sampling frequencies, parameters, and sampling amounts in the invention taught by Patel since this type of dynamic metrology would help to improve the quality of products and allow responses to changes in parameters which may cause a variance from intended target results in semiconductor manufacturing (Shanmugasundram, Paragraph 0012).

Referring to claims 15-17, see rejection of claims 7-9 above.

Referring to claim 18, Patel teaches a method, comprising: identifying at least one lot of wafers to be processed (col. 3 lines 5-6); identifying a process tool in which said at least one lot of wafers is to be processed (col. 4 lines 10-19);obtaining enhanced metrology data regarding a process operation to be performed in said identified process tool prior to processing said identified at least one wafer in said identified process tool (col. 3 lines 19-45, whereby feedback data containing any equipment disturbances is considered enhanced data); and positioning at least one wafer from said identified lot in said identified process tool and performing said process operation thereon (col. 3 lines 5-18). However, Patel does not explicitly teach in response to the identification of said at least one lot of wafers and the identification of said process tool, increasing a frequency at which metrology data regarding a process operation to be performed in said identified process tool is acquired prior to processing said identified at least one lot of wafers in said identified process tool.

Shanmugasundram teaches a method for dynamically altering sampling schemes in a semiconductor processing environment whereby different sampling frequencies can be varied in order to provide enhanced metrology data (Paragraph 0015 and Paragraphs 0037-0039).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to utilize different sampling frequencies in the invention taught by Patel since this type of dynamic metrology would help to improve the quality of products and allow responses to changes in parameters which may cause a variance from intended target results in semiconductor manufacturing (Shanmugasundram, Paragraph 0012).

Referring to claim 19, see rejection of claim 2 above.

Referring to claim 20, see rejection of claim 4 above.

Referring to claim 22, see rejection of claim 6 above.

Referring to claim 23, see rejection of claims 7-9 above.

Referring to claim 24, Patel teaches a method, comprising: identifying at least one lot of wafers to be processed (col. 3 lines 5-6); identifying a process tool in which said at least one lot of wafers is to be processed (col. 4 lines 10-19);obtaining enhanced metrology data regarding a process operation to be performed in said identified process tool prior to processing said identified at least one wafer in said identified process tool (col. 3 lines 19-45, whereby feedback data containing any equipment disturbances is considered enhanced data); and positioning at least one wafer from said identified lot in said identified process tool and performing said process operation thereon (col. 3 lines 5-18). However, Patel does not explicitly teach in response to the identification of said at least one lot of wafers and the identification of said process tool, increasing an amount of metrology data regarding a process operation to be performed in said identified process tool prior to processing said identified at least one lot of wafers in said identified process tool.

Shanmugasundram teaches a method for dynamically altering sampling schemes in a semiconductor processing environment whereby different amounts of sampling can be varied in order to provide enhanced metrology data (Paragraph 0015 and Paragraphs 0037-0039).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to utilize different amounts of sampling in the invention taught by Patel since this type of dynamic metrology would help to improve the quality of products and allow responses to changes in parameters which may cause a variance from intended target results in semiconductor manufacturing (Shanmugasundram, Paragraph 0012).

Referring to claim 25, see rejection of claim 2 above.

Referring to claim 26, see rejection of claim 4 above.

Referring to claim 28, see rejection of claim 6 above.

6) Claims 5 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel, further in view of Stoddard et al (U.S. Pat 6,587,744).

Referring to claim 5, Patel teaches the above. However, Patel does not explicitly teach the method of claim 1, wherein said identified at least one wafer is a test wafer.

Stoddard teaches a system comprising metrology tools and semiconductor processing tools whereby test wafers are used (col. 16 lines 15-25).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to utilize test wafers in the method taught by Patel since runs of processing tools utilizing test wafers can be utilized to obtain preliminary measurements to help build a preliminary model for process control (Stoddard, col. 16 lines 15-25).

Referring to claim 13, see rejection of claim 5 above.

7) Claims 21 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel, further in view of Shanmugasundram, further in view of Stoddard.

Referring to claim 21, see rejection of claim 5 above.

Referring to claim 27, see rejection of claim 5 above.

Conclusion

8) The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lin et al (U.S. Pat 6,594,536) – teaches a method of matching wafers to specific tools.

Noben et al (Cycle time advantages...) – teaches the use of integrated metrology and hot lots.

9) Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander J Kosowski whose telephone number is 571-272-3744. The examiner can normally be reached on Monday through Friday, alternating Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306. In addition, the examiner's RightFAX number is 571-273-3744.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Alexander J. Kosowski
Patent Examiner
Art Unit 2125

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

CLAIMS

WHAT IS CLAIMED:

1. A method, comprising:

identifying at least one wafer to be processed;

identifying a process tool in which said at least one wafer is to be processed;

obtaining enhanced metrology data regarding a process operation to be performed in said identified process tool prior to processing said identified at least one wafer in said identified process tool; and

positioning said at least one wafer in said identified process tool and performing said process operation thereon.

2. The method of claim 1, further comprising, prior to performing said process operation in said identified process tool, analyzing at least said enhanced metrology data to determine if said process tool is acceptable for processing said identified at least one wafer.

3. The method of claim 1, wherein said identified at least one wafer is part of a lot of wafers identified for processing in said identified process tool.

4. The method of claim 1, wherein said identified at least one wafer is a wafer wherein production integrated circuit devices are formed thereon.

5. The method of claim 1, wherein said identified at least one wafer is a test wafer.

6. The method of claim 1, wherein said identified process tool is at least one of a deposition tool, an etch tool, a furnace, an ion implant tool, a chemical mechanical polishing tool and a photolithography tool.

7. The method of claim 1, wherein said step of obtaining enhanced metrology data regarding said process operation comprises obtaining a greater amount of metrology data for said process operation relative to an amount of metrology data obtained for said process operation in accordance with a previously established metrology sampling plan.

8. The method of claim 1, wherein said step of obtaining enhanced metrology data regarding said process operation comprises obtaining a different type of metrology data for said process operation relative to a type of metrology data obtained for said process operation in accordance with a previously established metrology sampling plan.

9. The method of claim 1, wherein said step of obtaining enhanced metrology data regarding said process operation comprises increasing a frequency at which metrology data for said process operation is acquired relative to a frequency at which metrology data for said process operation is acquired in accordance with a previously established metrology sampling plan.

10. A method, comprising:

identifying at least one lot of wafers to be processed;

identifying a process tool in which said at least one lot of wafers is to be processed;

obtaining enhanced metrology data regarding a process operation to be performed in said identified process tool prior to processing said identified at least one lot of wafers in said identified process tool; and

positioning said at least one wafer from said identified lot of wafers in said identified process tool and performing said process operation thereon.

11. The method of claim 10, further comprising, prior to performing said process operation in said identified process tool, analyzing at least said enhanced metrology data to determine if said process tool is acceptable for processing said identified at least one wafer.

12. The method of claim 10, wherein said identified at least one lot of wafers is comprised of a plurality of wafers having production integrated circuit devices formed thereon.

13. The method of claim 10, wherein said identified at least one lot of wafers is comprised of a plurality of test wafers.

14. The method of claim 10, wherein said identified process tool is at least one of a deposition tool, an etch tool, a furnace, an ion implant tool, a chemical mechanical polishing tool and a photolithography tool.

15. The method of claim 10, wherein said step of obtaining enhanced metrology data regarding said process operation comprises obtaining a greater amount of metrology data for said process operation relative to an amount of metrology data obtained for said process operation in accordance with a previously established metrology sampling plan.

16. The method of claim 10, wherein said step of obtaining enhanced metrology data regarding said process operation comprises obtaining a different type of metrology data for said process operation relative to a type of metrology data obtained for said process operation in accordance with a previously established metrology sampling plan.

17. The method of claim 10, wherein said step of obtaining enhanced metrology data regarding said process operation comprises increasing a frequency at which metrology data for said process operation is acquired relative to a frequency at which metrology data for said process operation is acquired in accordance with a previously established metrology sampling plan.

18. A method, comprising:

identifying at least one lot of wafers to be processed;

identifying a process tool in which said at least one lot of wafers is to be processed;

in response to the identification of said at least one lot of wafers and the identification of said process tool, increasing a frequency at which metrology data regarding a process operation to be performed in said identified process tool is acquired prior to processing said identified at least one lot of wafers in said identified process tool; and

positioning at least one wafer from said identified lot in said identified process tool and performing said process operation thereon.

19. The method of claim 18, further comprising, prior to performing said process operation in said identified process tool, analyzing at least said metrology data acquired as a

result of the increased frequency at which metrology data is acquired to determine if said process tool is acceptable for processing said at least one lot of wafers.

20. The method of claim 18, wherein said identified at least one lot of wafers is comprised of a plurality of wafers wherein production integrated circuit devices are formed thereon.

21. The method of claim 18, wherein said identified at least one lot of wafers is comprised of a plurality of test wafers.

22. The method of claim 18, wherein said identified process tool is at least one of a deposition tool, an etch tool, a furnace, an ion implant tool, a chemical mechanical polishing tool and a photolithography tool.

23. The method of claim 18, wherein said step of increasing the frequency at which metrology data is acquired comprises obtaining a greater amount of metrology data for said process operation relative to an amount of metrology data obtained for said process operation in accordance with a previously established metrology sampling plan.

24. A method, comprising:

identifying at least one lot of wafers to be processed;

identifying a process tool in which said at least one lot of wafers is to be processed;

in response to the identification of said at least one lot of wafers and the identification of said process tool, increasing an amount of metrology data acquired regarding a process operation to be performed in said identified process tool prior to

processing said identified at least one lot of wafers in said identified process tool; and

positioning said at least one wafer from said identified lot of wafers in said identified process tool and performing said process operation thereon.

25. The method of claim 24, further comprising, prior to performing said process operation in said identified process tool, analyzing at least said increased amount of metrology data acquired to determine if said process tool is acceptable for processing said identified at least one wafer.

26. The method of claim 24, wherein said identified at least one lot of wafers is comprised of a plurality of wafers having production integrated circuit devices formed thereon.

27. The method of claim 24, wherein said identified at least one lot of wafers is comprised of a plurality of test wafers.

28. The method of claim 24, wherein said identified process tool is at least one of a deposition tool, an etch tool, a furnace, an ion implant tool, a chemical mechanical polishing tool and a photolithography tool.